AOZ23655QI

28V/18A VID Control Synchronous EZBuck™ Regulator

General Description

The AOZ23655QI is a high-efficiency, easy-to-use DC/DC synchronous buck regulators capable of operation from a 4V to 28V input bus. The device is capable of supplying 18A of continuous output current with an output voltage adjustment from 0V to 1.8V by controlling VID0 and VID1 signals.

A proprietary constant on-time PWM control with input feed-forward results in ultra-fast transient response while maintaining relatively constant switching frequency over the entire input voltage range.

The devices feature multiple protection functions such as V_{CC} under-voltage lockout, cycle-by-cycle current limit, output over-voltage protection, short-circuit protection, and thermal shutdown.

The AOZ23655QI is available in a 5mm×5mm QFN-31L package and is rated over a -40°C to +85°C ambient temperature range.

Features

- Wide input voltage range
  - 4V to 28V
- Support Intel I_{TDC} up to 18A
- Support Intel ICC_{MAX} up to 45A
- 2 bits programmable output voltage adjustable from 0V to 1.8V
- Integrated high performance trench MOSFETs capable of :
  - High peak current
    - Up to 90A with 10ms on pulse
    - Up to 120A with 10µs on pulse
  - Low RDS(ON) internal NFETs
    - 6.5mΩ high-side
    - 3mΩ low-side
- Constant On-Time with input feed-forward
- Programmable frequency up to 2.6µs
- Selectable PFM light load operation
- Adjustable load-line compensation
- High accuracy current monitor
- Remote sense
- Ceramic capacitor stable
- Fixed soft start
- Power Good output
- Integrated bootstrap diode
- Cycle-by-cycle current limit
- Short-circuit protection
- Over voltage protection
- Thermal shutdown
- Thermally enhanced 31-pin 5mm×5mm QFN

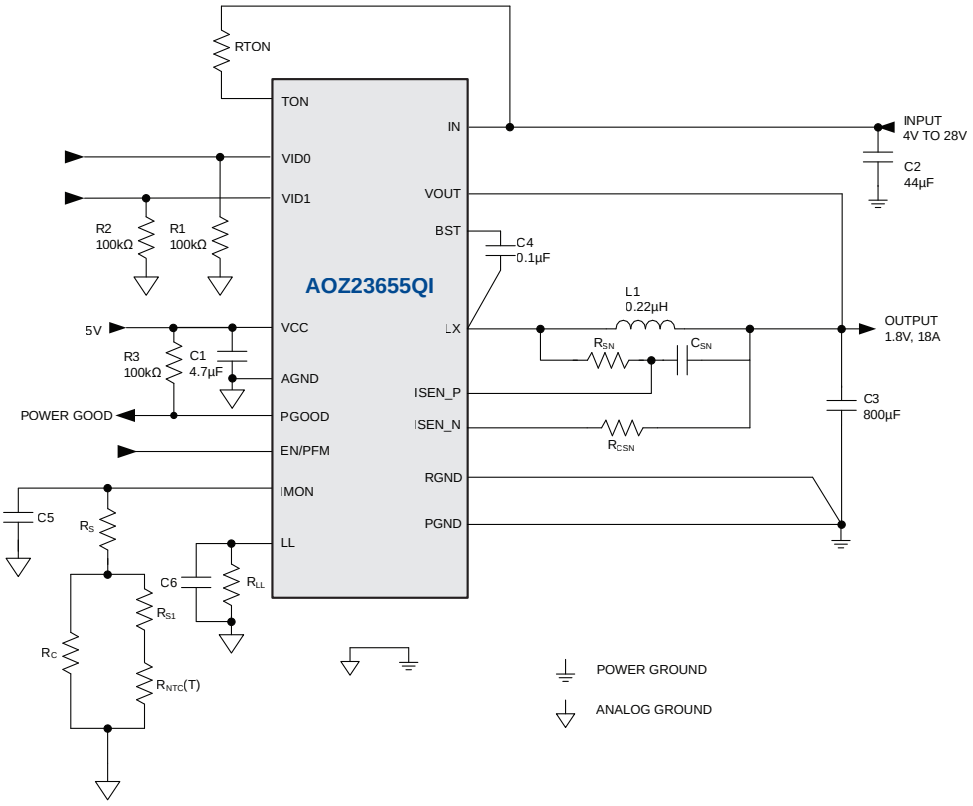
Applications

- Portable computers
- Compact desktop PCs
- Servers
- Networking equipment

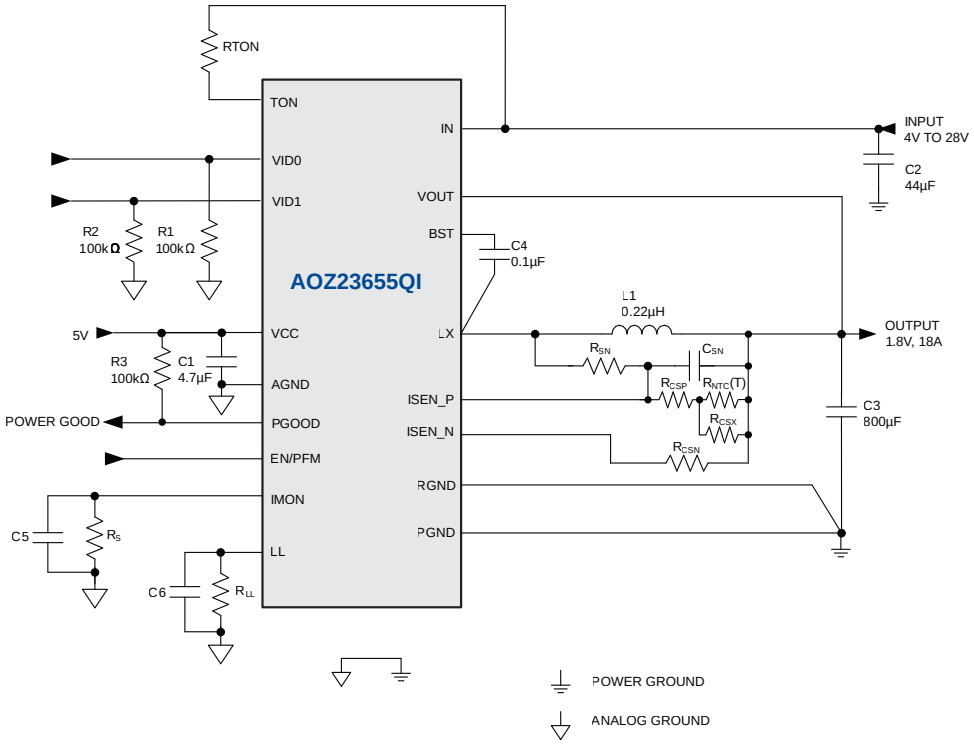
Green Product

Typical Application

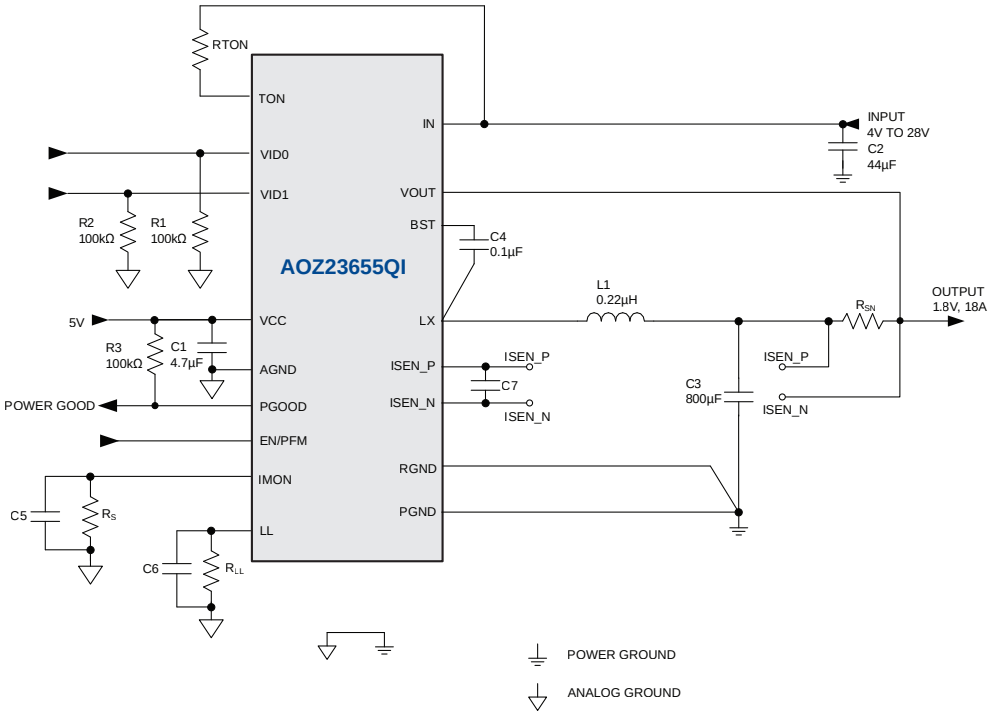
IMON 3rd Order Thermal Compensation Application
(Thermal Compensation only IMON Function)



IMON 2nd Order Thermal Compensation Application
(Thermal Compensation both LL and IMON Function)



IMON Application by Sensing Resistor

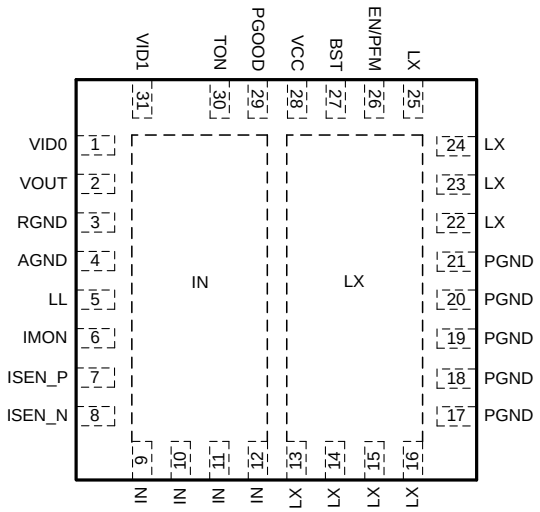


Ordering Information

Part Number	Temperature Range	Package	Environmental
AOZ23655QI	-40°C to +85°C	31-Pin 5×5 QFN	Green

AOS products are offered in packages with Pb-free plating and compliant to RoHS standards.
Please visit https://aosmd.com/sites/default/files/media/AOSGreenPolicy.pdf for additional information.

Pin Configuration



AOZ23655QI
31-pin 5mm x 5mm QFN

Pin Description

Pin Number	Pin Name	Pin Function
1	VID0	VID Interface.
2	VOUT	Output Voltage Feedback Input. Connection to the output voltage.
3	RGND	Remote Sensing GND. Connection to GND of the load.
4	AGND	Analog Ground.
5	LL	Loadline setting. Connect a resistor between LL and GND.
6	IMON	Current monitor output. The pin outputs a voltage which is proportional to the loading current.
7	ISEN_P	Positive current sense inputs. Connect to the most positive node of current sense resistor or inductor DCR sense R-C network.
8	ISEN_N	Negative current sense inputs. Connect to the most negative node of current sense resistor or inductor DCR sense R-C network.
9, 10, 11, 12	IN	Supply Input. IN is the regulator input. All IN pins must be connected together.
13, 14, 15, 16, 22, 23, 24, 25	LX	Switching Node.
17, 18, 19, 20, 21	PGND	Power Ground.
26	EN/PFM	Enable and PFM Selection Input. The AOZ23655QI is enabled when EN is pulled high. The device shuts down when EN is pulled low. Assert EN to high for power-up after IN and VCC are well supplied. The EN/PFM pin is less than 2.5V for PWM operation. The EN/PFM pin is larger than 2.5V for PFM operation.
27	BST	Bootstrap Capacitor Connection. The AOZ23655QI includes an internal bootstrap diode. Connect an external capacitor between BST and LX as shown in Typical Application diagram.
28	VCC	Supply input for analog functions and gate driver supply voltage for power stage. Connect a 5V supply capable of a minimum of 80mA. Bypass VCC to AGND with a 4.7µF~10µF ceramic capacitor. Place the capacitor close to VCC pin.
29	PGOOD	Power Good Signal Output. PGOOD is an open-drain output used to indicate the status of the output voltage. It is internally pulled low when the output voltage is 15% lower than the nominal regulation voltage for or higher than 2.2V. PGOOD is pulled low during soft-start and shut down.
30	TON	On-Time Setting Input. Connect a resistor between VIN and TON to set the on time.
31	VID1	VID Interface

Absolute Maximum Ratings

Exceeding the Absolute Maximum ratings may damage the device.

Parameter	Rating
IN, TON to AGND	-0.3V to 30V
IN to LX[1]	-0.3V to 30V
LX to AGND[2]	-1.0V to 30V
BST to AGND	-0.3V to 36V
TON to AGND	-0.3V to 30V
PGND to AGND	-0.3V to +0.3V
Other Pins to AGND	-0.3V to 6V
Junction Temperature (T_J)	+150°C
Storage Temperature (T_S)	-65°C to +150°C
ESD Rating-HBM[3]	2kV
ESD Rating-CDM	1kV

Notes:

1. IN to LX Transient (t<20ns) ----- -7V to VIN+7V.
2. LX to PGND Transient (t<20ns) ----- -7V to VIN+7V.
3. Devices are inherently ESD sensitive, handling precautions are required. Human body model rating: 1.5kΩ in series with 100pF.

Recommended Operating Conditions

The device is not guaranteed to operate beyond the Maximum Recommended Operating Conditions.

Parameter	Rating
Supply Voltage (V_{IN})	4V to 28V
Output Voltage Range	0V to 1.8V
Ambient Temperature (T_A)	-40°C to +85°C
Operating Junction Temperature (T_J)	-40°C to +145°C
Package Thermal Resistance (θ_{JA}) (θ_{JC})	 30°C/W 2.8°C/W

Electrical Characteristics

T_A = 25°C, V_{IN}=24V, EN = 5V, unless otherwise specified. Specifications in BOLD indicate a temperature range of -40°C to +85°C.

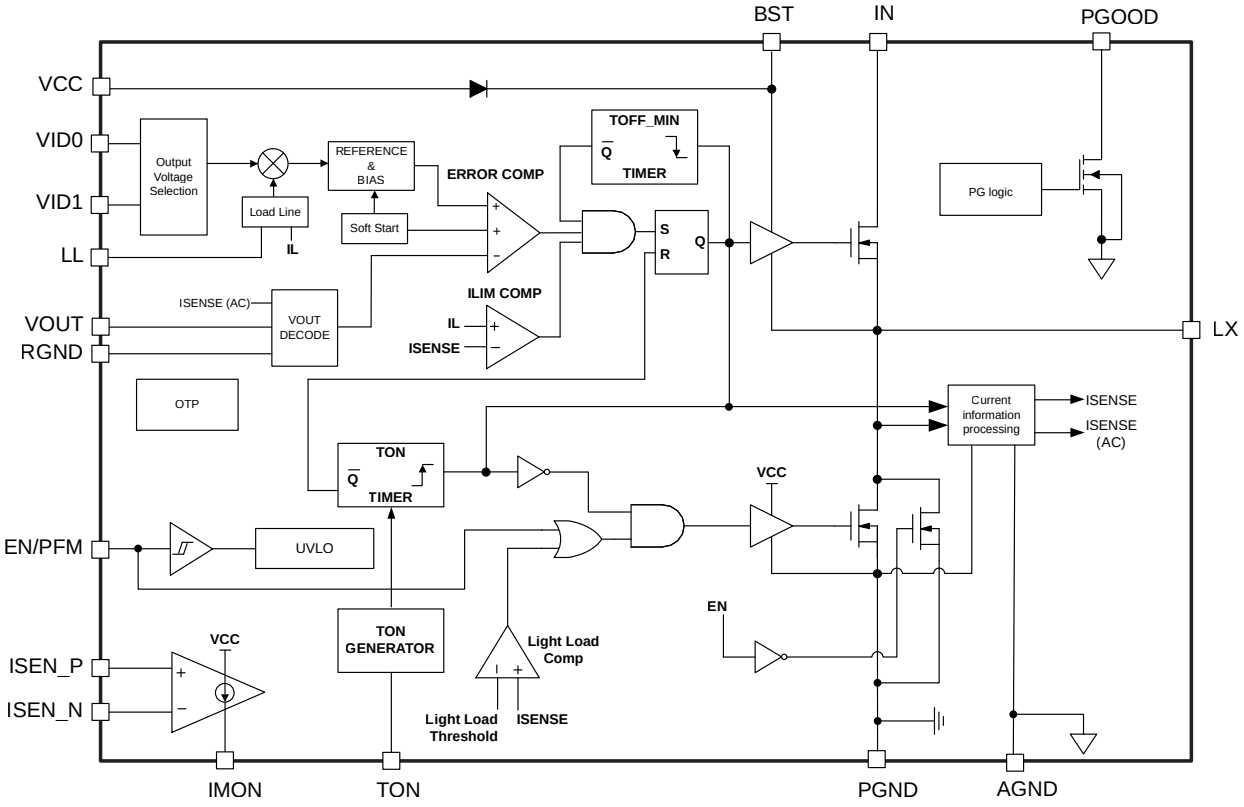
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IN}	IN Supply Voltage		**4**		**28**	V
V_{UVLO}	Under-Voltage Lockout Threshold of VCC	V_{CC} rising V_{CC} falling		**4.5** **4.1**		V
I_{SLEEP}	Sleep Mode Supply Current of V_{CC}	I_{OUT} = 0A, V_{EN} > 2V, VID[1,0]=00		**70**	**100**	µA
I_{OFF}	Shutdown Supply Current	V_{EN} = 0V		**1**	**2**	µA
I_{VOUT}	Output Voltage	VID[1,0]=00		0		V
		VID[1,0]=01		1.1		
		VID[1,0]=10		1.65		
		VID[1,0]=11		1.8		
T_{RAMP_UP}	Ramp up Time				149	µs
T_{RAMP_DOWN}	Ramp down Time	Does not apply for Decay mode			149	µs
VID 0 and VID 1						
V_{ID}	VID 0&VID1 Input Threshold	Low threshold High threshold	 2.0		0.3	V
V_{ID_HYS}	VID 0&VID1 Input Hysteresis			300		mV
Modulator						
f_{SW}	Operating Frequency	RTON=120kΩ		600		kHz

Electrical Characteristics

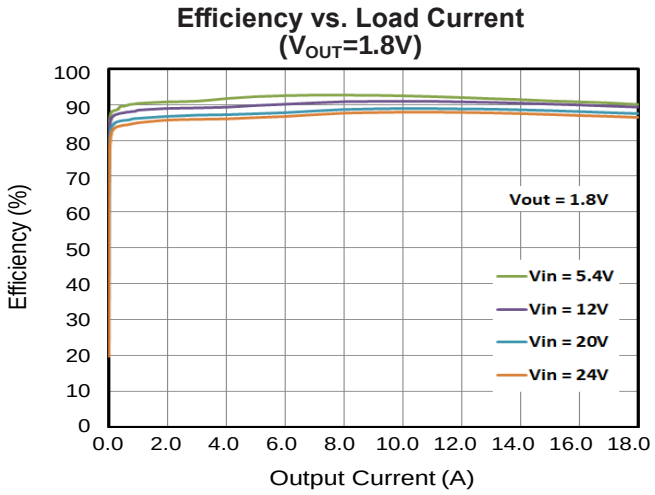
T_A = 25°C, V_{IN}=24V, EN = 5V, unless otherwise specified. Specifications in BOLD indicate a temperature range of -40°C to +85°C.

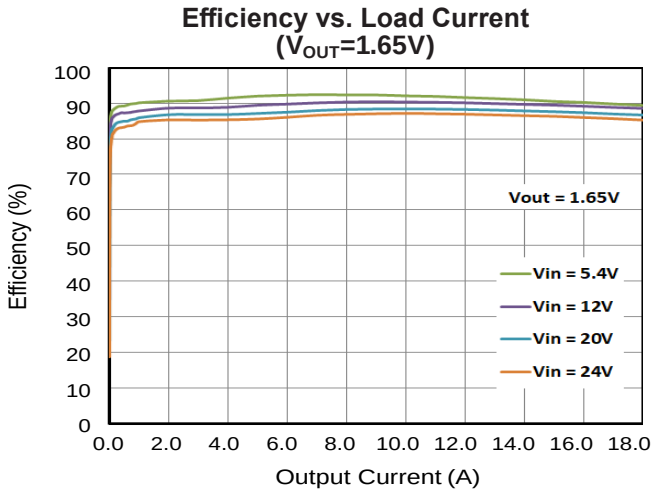
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Modulator						
T_{ON}	Normal On Time	V_{IN}=12V, VID[1,0]=01		150		ns
		V_{IN}=12V, VID[1,0]=10		230		
		V_{IN}=12V, VID[1,0]=11		250		
T_{ON_MIN}	Minimum On Time			70		
T_{OFF_MIN}	Minimum Off Time			400		
Soft-Start						
T_{SS_OUT}	SS time	For PGOOD signal is pulled high.		1.5		ms
Power Good Signal						
V_{PG_LOW}	PGOOD Low Voltage	I_{OL} = 1mA			0.5	V
	PGOOD Leakage Current				±1	µs
V_{PGH}	PGOOD Threshold (Low level to High level)	VOUT rising		90		%
V_{PGL}	PGOOD Threshold (High level to Low level)	VOUT rising (over 5µs) VOUT falling		2.2 85		V %
	PGOOD Threshold Hysteresis			5		%
T_{PG_DB}	De-bounce Time for PGOOD	PGOOD signal from low to high		20	30	µs
Under Voltage and Over Voltage Protection						
V_{PL}	Under Voltage threshold	VOUT falling		50		%
V_{PH}	Over Voltage Threshold	VOUT rising		2.2		V
Power Stage Output						
$R_{DS(ON)}$	High-Side NFET On- Resistance	V_{IN} = 12V, V_{CC} = 5V		6.5		mΩ
	High-Side NFET Leakage	V_{EN} = 0V, V_{LX} = 0			10	µA
$R_{DS(ON)}$	Low-Side NFET On- Resistance	V_{LX} = 12V, V_{CC} = 5V		3		mΩ
	Low-Side NFET Leakage	V_{EN} = 0V			10	µA
Enable						
V_{EN}	EN Input Threshold	Off threshold On threshold	 1.3		0.6	V
V_{EN_HYS}	EN Input Hysteresis			300		mV
Over-current and Thermal Protection						
I_{LIM_SC}	Source Current Limit	V_{CC} = 5V	55			A
I_{LIM_Sk}	Sink Current Limit	V_{CC} = 5V	24			A
	Thermal Shutdown Threshold	T_J rising		150		°C

Functional Block Diagram



Typical Performance Characteristics

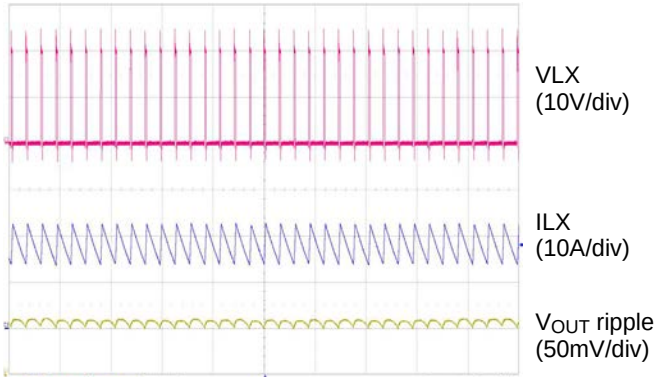




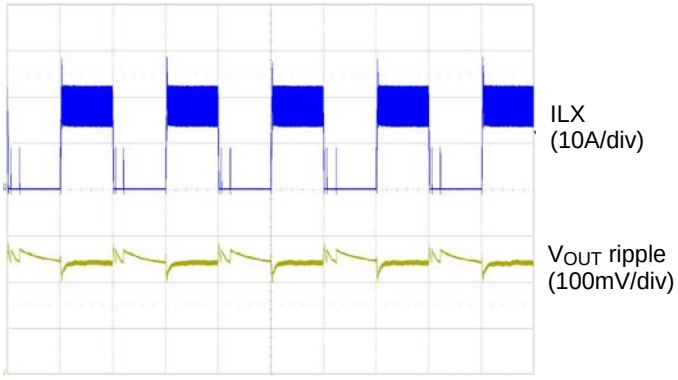
Typical Performance Characteristics

T_A = 25°C, V_{IN} = 20V, V_{OUT} = 1.8V, (VID[1:0]=11), L=0.22µH, unless otherwise specified.

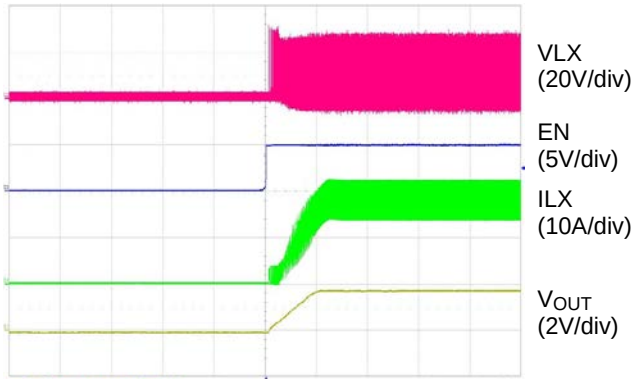
Normal Operation



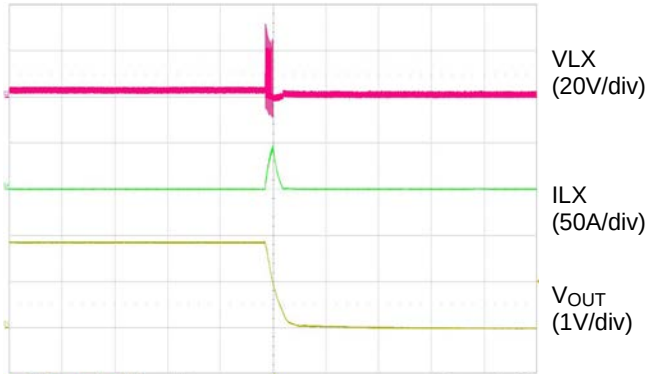
Load Transient 0A to 18A



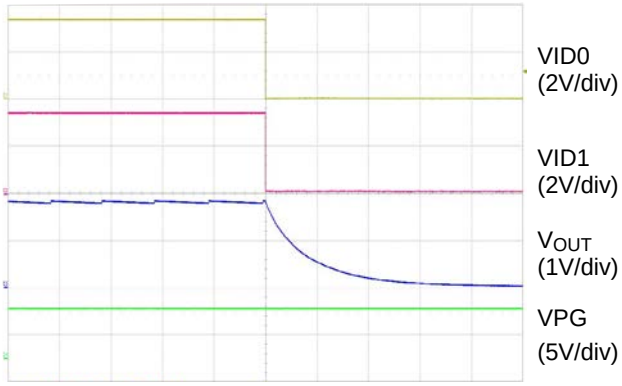
Full Load Start-up



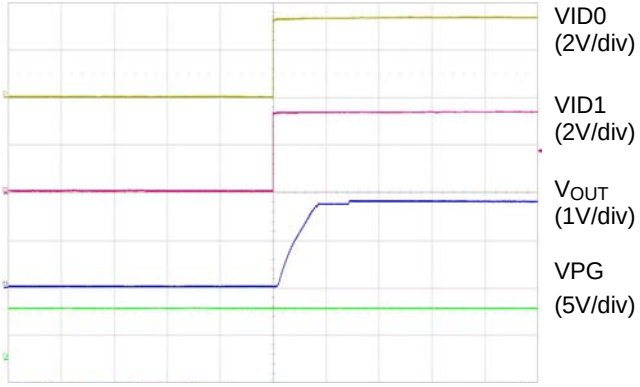
Short Circuit Protection



VID Change 1.8V to 0V



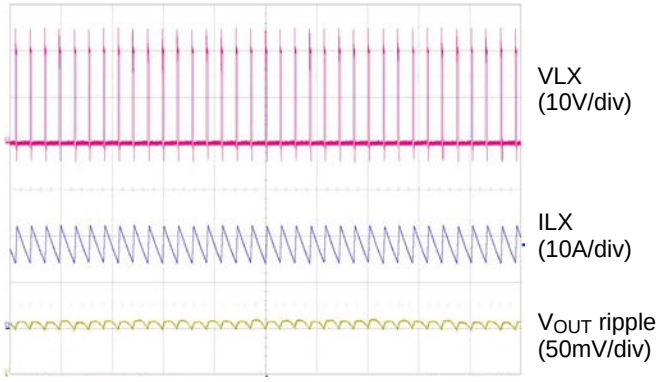
VID Change 0V to 1.8V



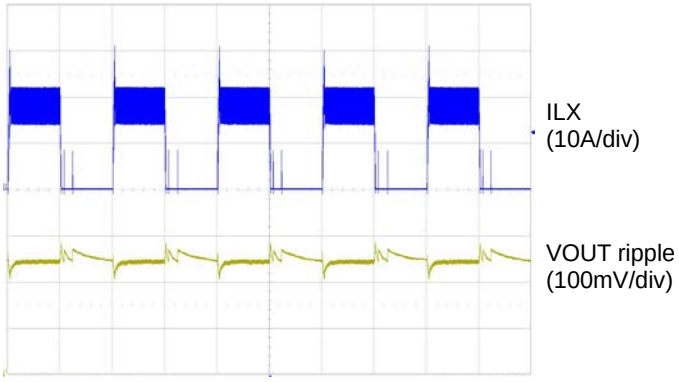
Typical Performance Characteristics

T_A = 25°C, V_{IN} = 20V, V_{OUT} = 1.65V, (VID[1:0]=10), L=0.22µH, unless otherwise specified.

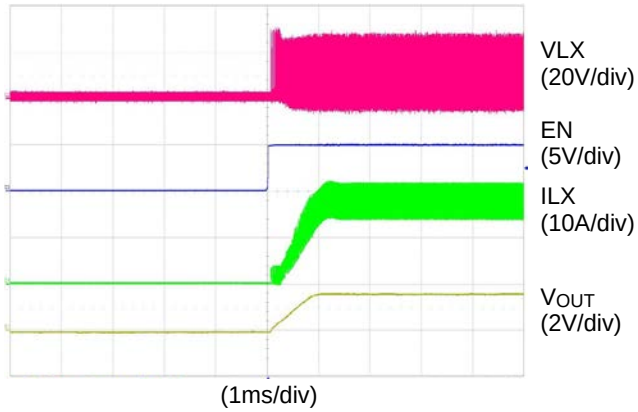
Normal Operation



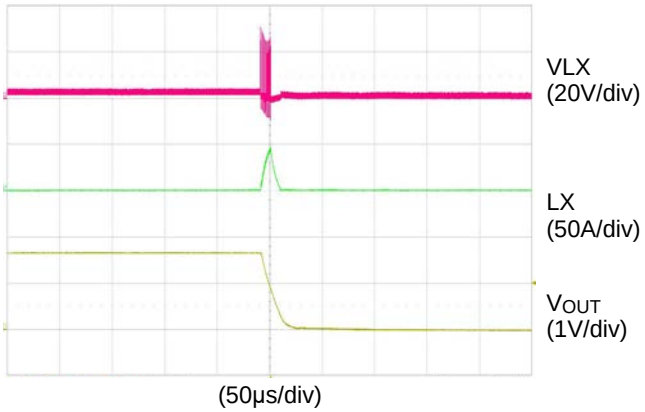
Load Transient 0A to 18A



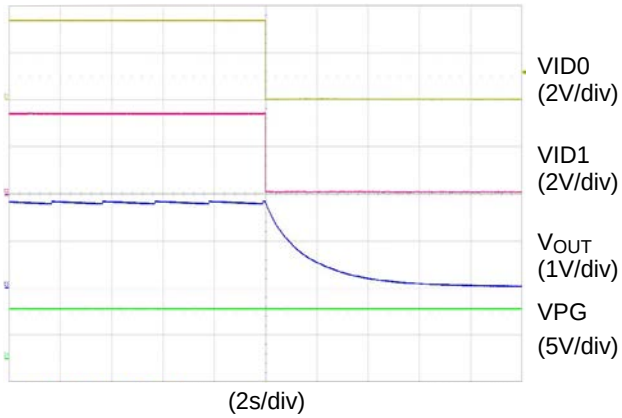
Full Load Start-up



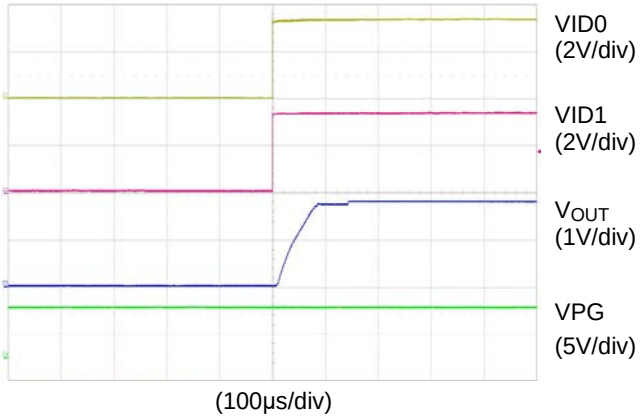
Short Circuit Protection



VID Change 1.65V to 0V



VID Change 0V to 1.65V



Detailed Description

The AOZ23655QI is a high-efficiency, easy-to-use DC/DC synchronous buck regulators capable of operation from a 4V to 28V input bus. The device is capable of supplying 18A of continuous output current with an output voltage adjustment from 0V to 1.8V by controlling VID0 and VID1 signals.

Constant on-time PWM with input feed-forward control scheme results in ultra-fast transient response while maintaining relatively constant switching frequency over the entire input range. True AC current mode control scheme guarantees the regulators can be stable with ceramics output capacitor. Protection features include V_{CC} under-voltage lockout, cycle-by-cycle current limit, output over voltage and under voltage protection, short-circuit protection, and thermal shutdown.

The AOZ23655QI is available in 31-pin 5mm×5mm QFN package.

Enable and Soft Start

The AOZ23655QI has internal soft start feature to limit in-rush current and ensure the output voltage ramps up smoothly to regulate voltage. A soft start process begins when V_{CC} rises to 4.5V and voltage on EN pin is HIGH. The output voltage follows the internal voltage of soft-start (V_{SS}) when it is lower than initial output voltage. When V_{SS} is higher than initial output voltage, the voltage of VOUT pin is regulated by internal precise band-gap voltage. Moreover, the soft start period between EN and PGOOD is 1.5ms. The soft start sequence of AOZ23655QI is shown in Figure 1.

The AOZ23655QI has the auto-skip mode control function to achieve higher efficiency at light load condition. When the output current decreases, the inductor current also reduces. If the inductor current valley point reaches to zero current, the AOZ23655QI operates at auto-skip mode. It means the zero current is the boundary between pulse-width mode and auto-skip mode. As the inductor current reaches to zero current, the low-side MOSFET is turned off, and then the AOZ23655QI operates at tri-state for auto-skip mode. Until output voltage is less than reference voltage, the on time signal is triggered to turn on high-side MOSFET.

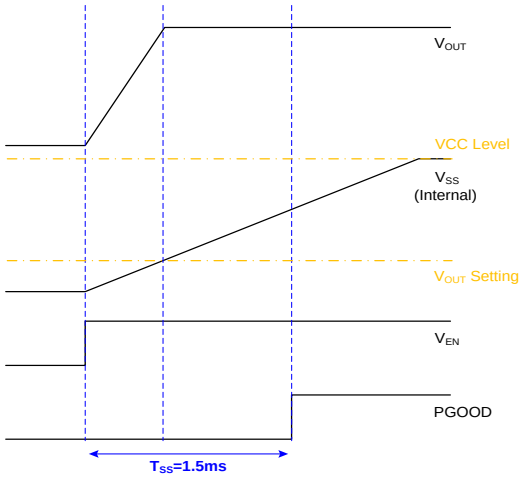


Figure 1. Soft Start Sequence of AOZ23655QI

The EN/PFM pin provides the 3 different levels of EN and PFM for flexible design. Table 1 shows the recommended voltage for corresponding mode.

Table 1. EN/PFM Pin Voltage for Corresponding Setting

State	EN/PFM Pin Voltage	Condition
Mode 1	EN/PFM pin<1.3V	EN Disable
Mode 2	1.3V<EN/PFM pin<2.5V	EN Enable and PWM Mode
Mode 3	EN/PFM pin>2.5V	EN Enable and PFM Mode

Constant-On-Time PWM Control with Input Feed-Forward

The control algorithm of AOZ23655QI is constant-on-time PWM Control with input feed-forward.

The simplified control schematic is shown in Figure 2. The high-side switch on-time is determined solely by a one-shot whose pulse width is inversely proportional to input voltage (IN). The one-shot is triggered when the internal setting output voltage is higher than the combined information of output voltage and the AC current information of inductor and load line signal, which is processed and obtained through the sensed low-side MOSFET current once it turns-on. The added AC current information can help the stability of constant-on time control even with pure ceramic output capacitors, which have very low ESR. The AC current information has no DC offset, which does not cause offset with output load change, which is fundamentally different from other V^2 constant-on time control schemes.

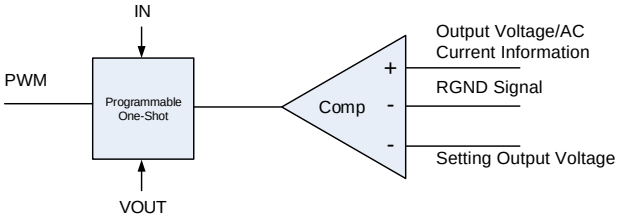


Figure 2. Simplified Control Schematic of AOZ23655QI

The constant-on-time PWM control architecture is a pseudo-fixed frequency with input voltage feed-forward. The internal circuit of AOZ23655QI sets the on-time of high-side switch inversely proportional to the IN.

$$T_{on} \propto \frac{R_{ton}(\Omega)}{V_{in}(V)} \quad (1)$$

To achieve the flux balance of inductor, the buck converter has the equation:

$$F_{sw} = \frac{V_{out}}{V_{in} * T_{on}} \quad (2)$$

Once the product of Vin*Ton is constant, the switching frequency keeps constant and is independent of input voltage.

An external resistor between the IN and TON pins sets the switching on-time according to the following curves:

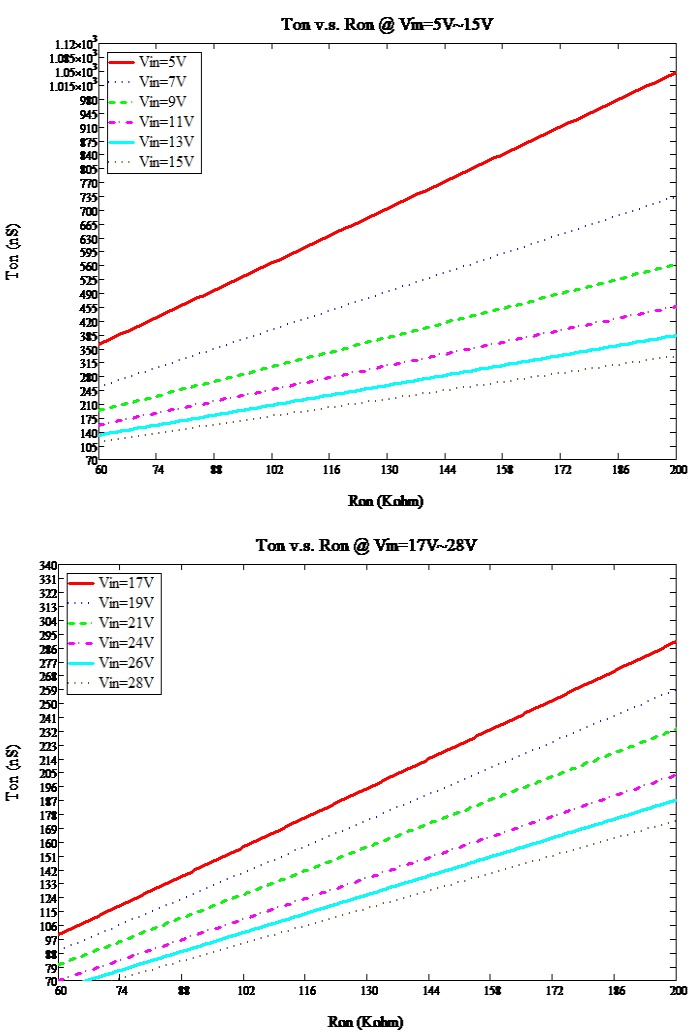


Figure 3. Ton vs. Rton Curves for AOZ23655QI

A further simplified equation will be

$$F_{sw}(KHz) = \frac{V_{out}(V)}{V_{in}(V) \cdot T_{on}(ns)} \cdot 10^6 \quad (4)$$

If V_{out} is 1.8V, Vin is 13V, and set Fs=600kHz. According to eq.(4), Ton=230ns is needed. Finally, use the Ton to Ron curve, we can find out Ron is 120kΩ.

This algorithm results in a nearly constant switching frequency despite the lack of a fixed-frequency clock generator.

When the switching frequency is fixed at V_{out}=1.8V, the switching frequency of other output voltage level is also fixed to the same switching frequency as V_{out}=1.8V one.

The required ICC current capability is related to the switching frequency. Below shows the required ICC capability curve for different switching frequencies:

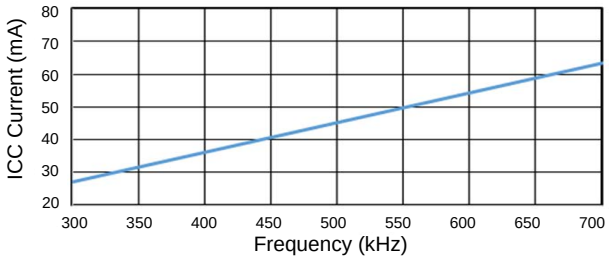


Figure 4. Required ICC Capability vs. Frequency

True Current Mode Control

The constant-on-time control scheme is intrinsically unstable if output capacitor's ESR is not large enough as an effective current-sense resistor. Ceramic capacitors usually cannot be used as output capacitor.

The AOZ23655QI senses the low-side MOSFET current and processes it into DC current and AC current information using AOS proprietary technique. The AC current information is decoded and added on the FB pin on phase. With AC current information, the stability of constant-on-time control is significantly improved even without the help of output capacitor's ESR; and thus the pure ceramic capacitor solution can be applicant. The pure ceramic capacitor solution can significantly reduce the output ripple (no ESR caused overshoot and undershoot) and less board area design.

Decay Mode

The AOZ23655QI has the decay mode function to implement power saving when there are frequent transitions from higher output voltage to lower one, the regulator output stops switching and goes high impedance. The output naturally decays into the load. The decay mode illustration is shown in Figure 5.

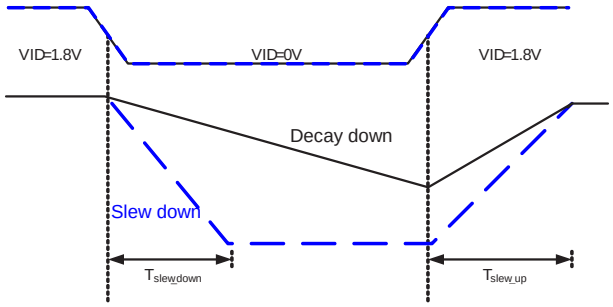


Figure 5. Decay Mode Illustration

2 Bits Programmable VID

The AOZ23655QI implements an output voltage adjustment by controlling VID0 and VID1 signals. Table 2 shows the output voltage for corresponding VID setting.

Table 2. Output Voltage for Corresponding VID Setting

VOUT Setting	VID0	VID1
1.8V	1	1
1.65V	0	1
1.1V	1	0
0V	0	0

Current Monitor

The AOZ23655QI includes a current monitor (IMON) function. The current monitor puts out an analog voltage proportional to the output current on the IMON pin. The current monitor function is determined with the DCR sensing circuit. Considering the DCR thermal effect, the IMON circuit uses the NTC resistor to improve the IMON accuracy to cover the DCR variation.

Load-Line

The load-line function can be set by load-line resistor. Load-line is used to save on output capacitor and improve the overshoot/undershoot at load transient condition.

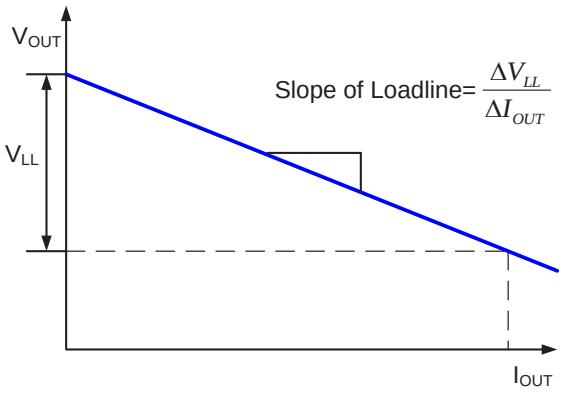


Figure 6. Load-line Illustration

Remote sensing Function

The AOZ23655QI provides the remote sensing function to implement better load regulation in high current application. The VOUT and RGND pins need to connect to the load terminal by kelvin-sensing method. It can compensate the voltage drop from PCB ESR to the setting output voltage that we want. The remote sensing traces (VOUT and RGND return trace) should be far away against from switching signals and high current paths on PCB application. Figure 7 shows the remote sensing connection.

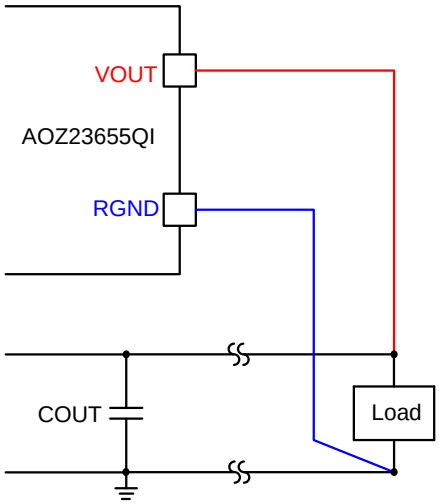


Figure 7. Remote Sensing Connection

Current-Limit Protection

The AOZ23655QI has the current-limit protection by using R_{dson} of the low-side MOSFET to be as current sensing. To detect real current information, a minimum constant off time (400ns typical) is implemented after a constant-on time. If the current exceeds the current-limit threshold, the PWM controller is not allowed to initiate a new cycle. The actual peak current is greater than the current-limit threshold by an amount equal to the inductor ripple current. Therefore, exact

current-limit characteristic and maximum load capability are a function of the inductor value and input and output voltages. The current limit will keep the low-side MOSFET on and will not allow another high-side on-time, until the current in the low-side MOSFET reduces below the current limit.

After 16 switching cycles, the AOZ23655QI considers this is a true failed condition and thus turns-off both high-side and low-side MOSFET and latches off. Only trigger the enable again can restart the AOZ23655QI.

Output Voltage Under-voltage Protection

If the output voltage is lower than 50% by over-current or short circuit, AOZ23655QI turns-off both high-side and low-side MOSFET and latches off. Only trigger the enable again can restart the AOZ23655QI.

Output Voltage Over-voltage Protection

The threshold of OVP is set on 2.2V. When the output voltage exceeds the OVP threshold, high-side and low-side MOSFET are turned-off. If the time is over 5µs for the output voltage is higher than the OVP threshold, AOZ23655QI is latched-off. Only trigger the enable again can restart the AOZ23655QI.

Power Good Output

The power good (PGOOD) output, which is an open drain output, requires the pull-up resistor. When the output voltage is 15% below than the nominal regulation voltage for, the PGOOD is pulled low. When the output voltage is higher than 2.2V, the PGOOD is also pull low.

When combined with the under-voltage-protection circuit, this current-limit method is effective in almost every circumstance.

Application Information

The basic AOZ23655QI application circuit is shown in Typical Application diagram. Component selection is explained below.

Input Capacitor

The input capacitor must be connected to the IN pins and PGND pin of the AOZ23655QI to maintain steady input voltage and filter out the pulsing input current. A small decoupling capacitor, usually 4.7uF, should be connected to the VCC pin and AGND pin for stable operation of the AOZ23655QI. The voltage rating of input capacitor must be greater than maximum input voltage plus ripple voltage.

The input ripple voltage can be approximated by equation below:

$$\Delta V_{IN} = \frac{I_{OUT}}{f \times C_{IN}} \times (1 - \frac{V_{OUT}}{V_{IN}}) \times \frac{V_{OUT}}{V_{IN}}$$

Since the input current is discontinuous in a buck converter, the current stress on the input capacitor is another concern when selecting the capacitor. For a buck circuit, the RMS value of input capacitor current can be calculated by:

$$I_{CIN\_RMS} = I_{OUT} \times \sqrt{\frac{V_{OUT}}{V_{IN}}(1 - \frac{V_{OUT}}{V_{IN}})}$$

if let m equal the conversion ratio:

$$\frac{V_{OUT}}{V_{IN}} = m$$

The relation between the input capacitor RMS current and voltage conversion ratio is calculated and shown in Figure 8 below. It can be seen that when V_{out} is half of V_{IN}, C_{IN} is under the worst current stress. The worst current stress on C_{IN} is $0.5 \cdot I_{out}$.

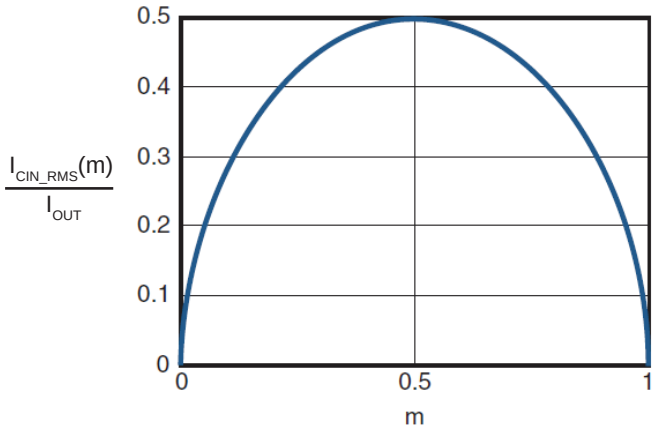


Figure 8. I_{CIN} vs. Voltage Conversion Ratio

For reliable operation and best performance, the input capacitors must have current rating higher than $I_{CIN-RMS}$ at worst operating conditions. Ceramic capacitors are preferred for input capacitors because of their low ESR and high ripple current rating. Depending on the application circuits, other low ESR tantalum capacitor or aluminum electrolytic capacitor may also be used. When selecting ceramic capacitors, X5R or X7R type dielectric ceramic capacitors are preferred for their better temperature and voltage characteristics. Note that the ripple current rating from capacitor manufactures is based on certain amount of life time. Further de-rating may be necessary for practical design requirement.

Inductor

The inductor is used to supply constant current to output when it is driven by a switching voltage. For given input and output voltage, inductance and switching frequency together decide the inductor ripple current, which is,

$$\Delta I_L = \frac{V_{OUT}}{f \times L} \times (1 - \frac{V_{OUT}}{V_{IN}})$$

The peak inductor current is:

$$I_{Lpeak} = I_{OUT} + \frac{\Delta I_L}{2}$$

High inductance gives low inductor ripple current but requires larger size inductor to avoid saturation. Low ripple current reduces inductor core losses. It also reduces RMS current through inductor and switches, which results in less conduction loss. Usually, peak to peak ripple current on inductor is designed to be 30% to 50% of output current.

When selecting the inductor, make sure it is able to handle the peak current without saturation even at the highest operating temperature.

AOZ23655QI is designed for fast transient application, like VRTT testing. So 0.22µH and 0.15µH inductance is the best choice. For better IMON accuracy, the inductor DCR must be larger than 2.3mΩ.

The inductor takes the highest current in a buck circuit. The conduction loss on inductor needs to be checked for thermal and efficiency requirements.

Surface mount inductors in different shape and styles are available from Coilcraft, Elytone and Murata. Shielded inductors are small and radiate less EMI noise. But they cost more than unshielded inductors. The choice depends on EMI requirement, price and size.

Output Capacitor

The output capacitor is selected based on the DC output voltage rating, output ripple voltage specification and ripple current rating.

The selected output capacitor must have a higher rated voltage specification than the maximum desired output voltage including ripple. De-rating needs to be considered for long term reliability.

Output ripple voltage specification is another important factor for selecting the output capacitor. In a buck converter circuit, output ripple voltage is determined by inductor value, switching frequency, output capacitor value and ESR. It can be calculated by the equation below:

$$\Delta V_{OUT} = \Delta I_L \times (ESR_{COUT} + \frac{1}{8 \times f \times C_{OUT}})$$

where COUT is output capacitor value and ESRCOUT is the Equivalent Series Resistor of output capacitor.

When low ESR ceramic capacitor is used as output capacitor, the impedance of the capacitor at the switching frequency dominates. Output ripple is mainly caused by capacitor value and inductor ripple current. The output ripple voltage calculation can be simplified to:

$$\Delta V_{OUT} = \Delta I_L \times \frac{1}{8 \times f \times C_{OUT}}$$

If the impedance of ESR at switching frequency dominates, the output ripple voltage is mainly decided by capacitor ESR and inductor ripple current. The output ripple voltage calculation can be further simplified to:

$$\Delta V_{OUT} = \Delta I_L \times ESR_{COUT}$$

For lower output ripple voltage across the entire operating temperature range, X5R or X7R dielectric type of ceramic, or other low ESR tantalum are recommended to be used as output capacitors.

In a buck converter, output capacitor current is continuous. The RMS current of output capacitor is decided by the peak to peak inductor ripple current. It can be calculated by:

$$I_{COUT\_RMS} = \frac{\Delta I_L}{\sqrt{12}}$$

Usually, the ripple current rating of the output capacitor is a smaller issue because of the low current stress. When the buck inductor is selected to be very small and inductor ripple current is high, output capacitor could be overstressed. The recommended output capacitance is 800uF for fast transient and VID change application. Larger output capacitance possible cause lager inrush current when VID change, therefore, output capacitance need to carefully estimate.

Power MOSFET SOA Curve

AOZ23655QI integrates AOS's state of the art Trench MOSFETs. Robust SOA ensures reliable operation in high performance buck regulator applications.

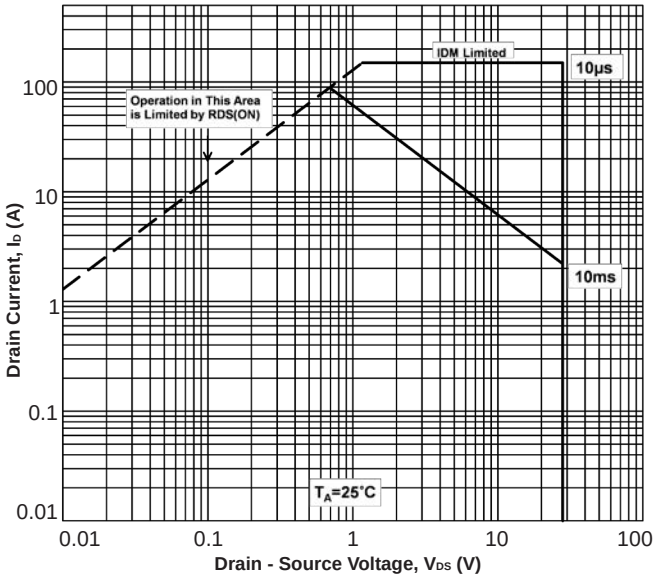


Figure 9. High-Side MOSFET SOA Curve

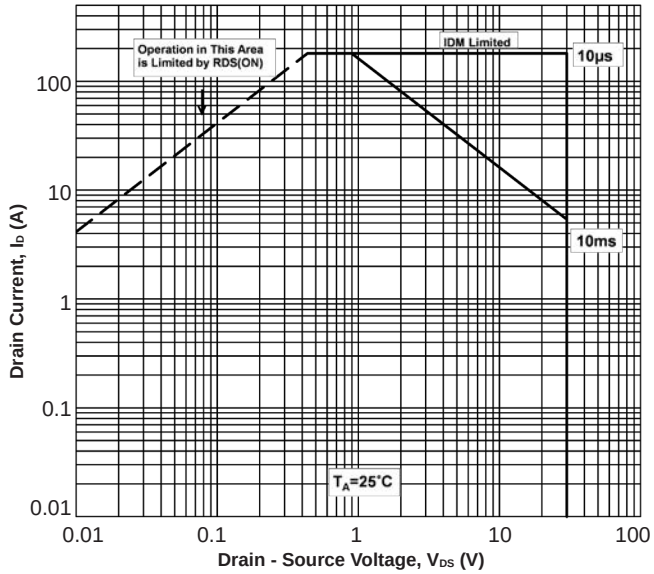


Figure 10. Low-Side MOSFET SOA Curve

Thermal Management and Layout Consideration

In the AOZ23655QI buck regulator circuit, high pulsing current flows through two circuit loops. The first loop starts from the input capacitors, to the VIN pin, to the LX pins, to the filter inductor, to the output capacitor and load, and then return to the input capacitor through ground. Current flows in the first loop when the high side switch is on. The second loop starts from inductor, to the output capacitors and load, to the low side switch. Current flows in the second loop when the low side low side switch is on.

In PCB layout, minimizing the two loops area reduces the noise of this circuit and improves efficiency. A ground plane is strongly recommended to connect input capacitor, output capacitor, and PGND pin of the AOZ23655QI.

In the AOZ23655QI buck regulator circuit, the major power dissipating components are the AOZ23655QI and the output inductor. The total power dissipation of converter circuit can be measured by input power minus output power.

$$P_{total\_loss} = V_{IN} \cdot I_{IN} - V_{OUT} \cdot I_{OUT}$$

The power dissipation of inductor can be approximately calculated by DCR of inductor and output current.

$$P_{inductor\_loss} = I_{OUT}^{2} \cdot R_{inductor} \cdot 1.1$$

The actual junction temperature can be calculated with power dissipation in the AOZ23655QI and thermal impedance from junction to ambient. $T_{junction} = (P_{total\_loss} - P_{inductor\_loss}) \cdot \theta_{JA} + T_A$

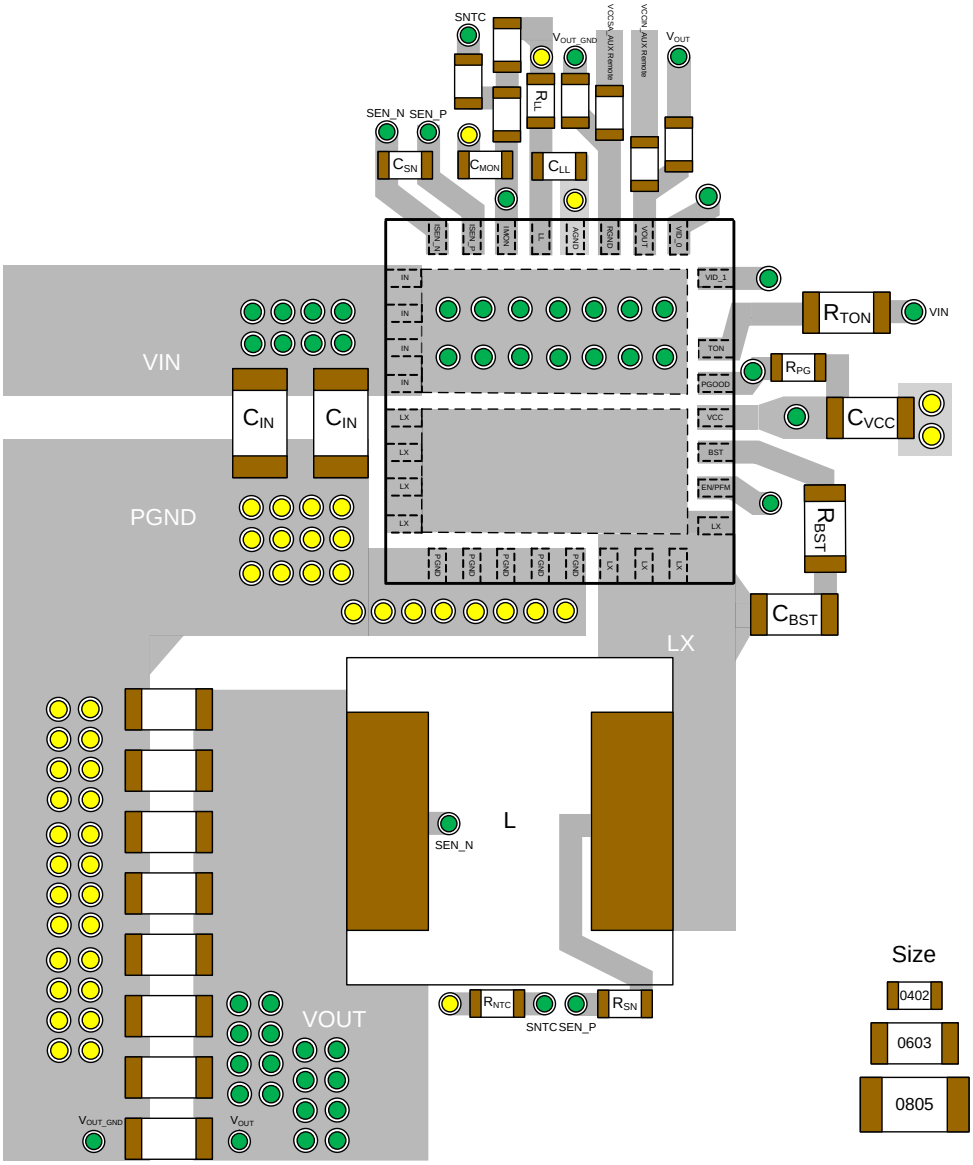
The maximum junction temperature of AOZ23655QI is 150ºC, which limits the maximum load current capability.

The thermal performance of the AOZ23655QI is strongly affected by the PCB layout. Extra care should be taken by users during design process to ensure that the IC will operate under the recommended environmental conditions.

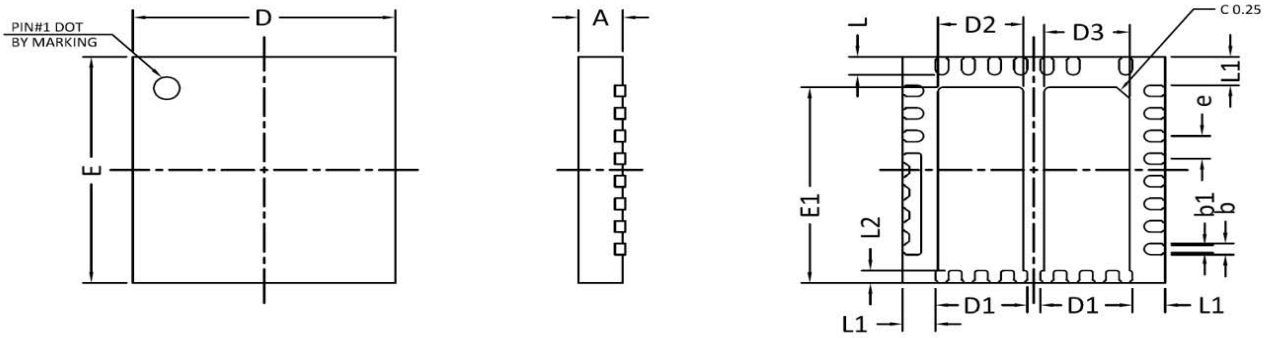
Layout Considerations

Several layout tips are listed below for the best electric and thermal performance.

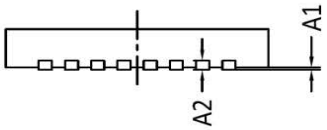
1. Connected a small copper plane to LX pin to have lower noise interference area.
2. The IN pins and pad are connected to internal high side switch drain. They are also low resistance thermal conduction path. Connected a large copper plane to IN pins to help thermal dissipation.
3. Input capacitors should be connected to the IN pin and the PGND pin as close as possible to reduce the switching spikes.
4. Decoupling capacitor CVCC should be connected to VCC and AGND as close as possible.
5. DCR sensing capacitor CSN should be connected to ISEN_P and ISEN_N as close as possible.
6. Keep sensitive signal traces such as output trace and RGND trace far away from the LX pins.
7. Let VID0, VID1, LL, and IMON pin to use AGND Pour copper plane on all unused board area and connect it to stable DC nodes, like VIN, GND or VOUT.
8. Do not connect the LX plane by any VIAS to avoid the noise couple.
9. The GND terminal of VCC decoupling capacitor, should be single connect to GND plane by VIAS.



Package Dimensions, QFN5x5-31L

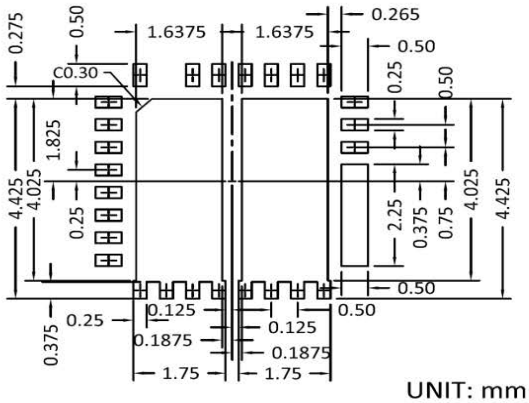


TOP VIEW SIDE VIEW BOTTOM VIEW



SIDE VIEW

RECOMMENDED LAND PATTERN



UNIT: mm

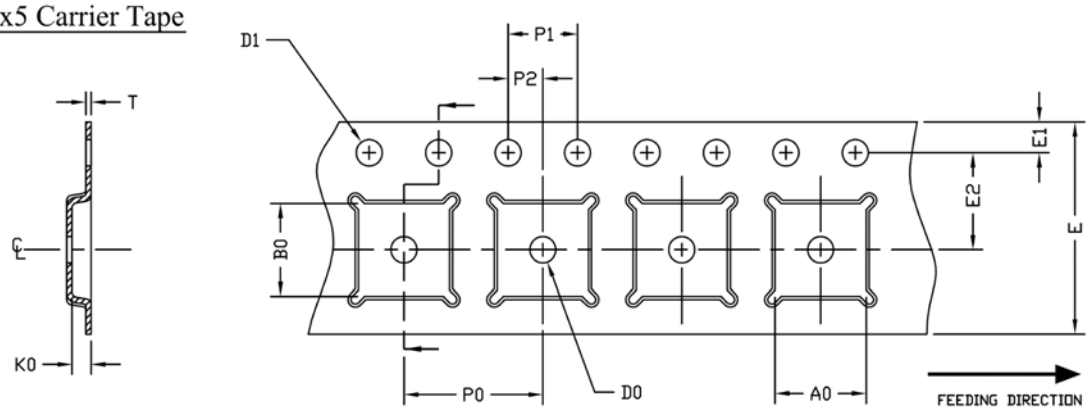
SYMBOLS	DIMENSION IN MM			DIMENSION IN INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.80	0.90	1.00	0.031	0.035	0.039
A1	0.00	---	0.05	0.000	----	0.002
A2		0.2REF			0.008REF	
E	4.90	5.00	5.10	0.193	0.197	0.201
E1	4.22	4.32	4.42	0.166	0.170	0.174
D	4.90	5.00	5.10	0.193	0.197	0.201
D1	1.65	1.75	1.85	0.065	0.069	0.073
D2	1.53	1.63	1.73	0.060	0.064	0.068
D3	1.53	1.63	1.73	0.060	0.064	0.068
L	0.35	0.40	0.45	0.014	0.016	0.018
L1	0.57	0.62	0.67	0.022	0.024	0.026
L2	0.225	0.275	0.325	0.009	0.011	0.013
b	0.20	0.25	0.30	0.008	0.010	0.012
e		0.50 BSC			0.020BSC	

NOTE：

1. CONTROLLING DIMENSION IS MILLIMETER.
   CONVERTED INCH DIMENSIONS ARE NOT NECESSARILY EXACT.
2. TOLERANCE :±0.05 UNLESS OTHERWISE SPECIFIED.
3. RADIUS ON ALL CORNER ARE 0.152 MAX, UNLESS OTHERWISE SPECIFIED.
4. PACKAGE WARPAGE: 0.012 MAX.
5. PAD PLANARITY: ±0.102.

Tape and Reel Dimensions, QFN5x5, 31L

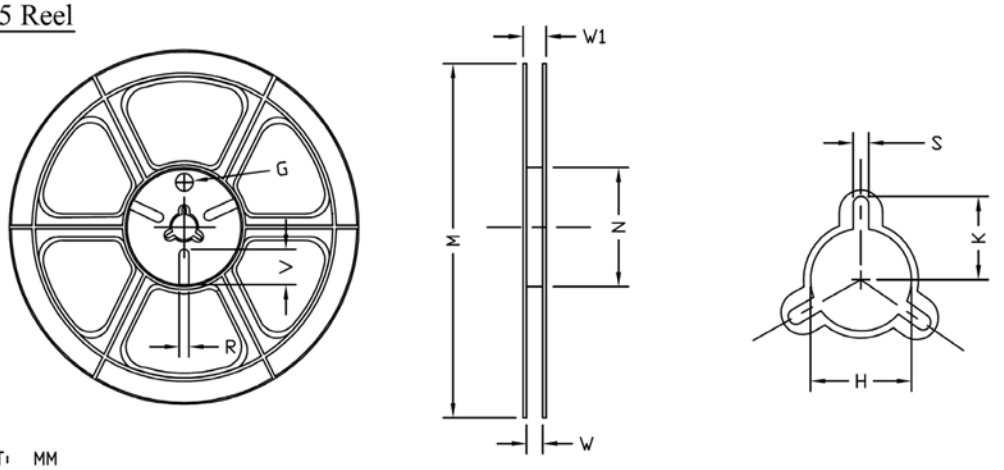
QFN5x5 Carrier Tape



UNIT: MM

PACKAGE	A0	B0	K0	D0	D1	E	E1	E2	P0	P1	P2	T
QFN5x5 (12 mm)	5.25 ±0.10	5.25 ±0.10	1.10 ±0.10	1.50 MIN.	1.50 +0.1 −0.0	12.0 ±0.3	1.75 ±0.10	5.50 ±0.05	8.00 ±0.10	4.00 ±0.10	2.00 ±0.05	0.30 ±0.05

QFN5x5 Reel

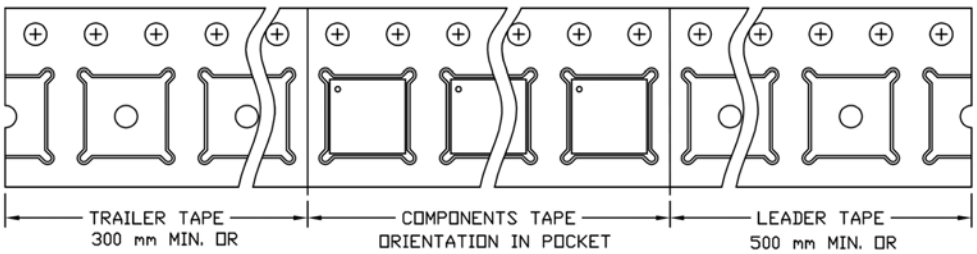


UNIT: MM

TAPE SIZE	REEL SIZE	M	N	W	W1	H	K	S	G	R	V
12 mm	ø330	ø330.0 ±2.0	ø100.0 ±1.0	12.4 +2.0 −0.0	17.0 +2.6 −1.2	ø13.0 ±0.5	10.5 ±0.2	2.0 ±0.5	---	---	---

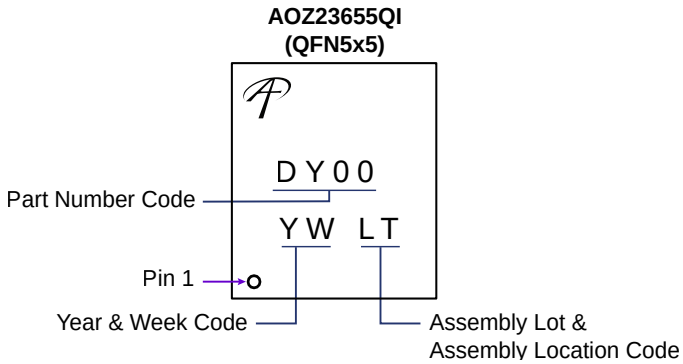
QFN5x5 Tape

Leader / Trailer & Orientation



Unit Per Reel: 3000pcs

Part Marking



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2. A critical component in any component of a life support, device, or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.